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First Named Inventor	Shogo Oneda
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Examiner Name	Yon Jung Couso
Attorney Docket Number	6453P008

ENCLOSURES *(check all that apply)*

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  - ☐ Fee Attached
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  - ☐ Affidavits/declaration(s)
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- ☒ Other Enclosure(s) *(please identify below):*

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Date	July 30, 2007

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[List of Attached Documents]

[Name of Document] Scope of Claims 1

[Name of Document] Specification 1

[Name of Document] Drawing 1

[Name of Document] Abstract 1

[Name of Document] Scope of Claims

[Claim 1]

An image decompression apparatus comprising:

a code decompression means for decompressing code data produced

Date of Filing: November 28, 2002
Japanese Patent Application No.: 2002-345237

[Name of Document] Application for Patent

[Reference No.] 200207431

[Date of Filing] November 28, 2002

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[List of Attached Documents]

[Name of Document] Scope of Claims 1

[Name of Document] Specification 1

[Name of Document] Drawing 1

[Name of Document] Abstract 1

[Name of Document] Scope of Claims

[Claim 1]

An image compression apparatus comprising:

an image compression means for compressing and encoding an image;

a detection means for detecting a battery remaining amount when

a power supply of the apparatus is a battery; and

a first setting means for setting a compression/encoding rate control mode in accordance with the detected battery remaining amount.

[Claim 2]

An image compression apparatus comprising:

an image compression means for dividing an image into a plurality of tiles and compressing and encoding an image in a hierarchical manner for each of the tiles;

a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery; and

a first setting means for setting a tiling mode in accordance with the detected battery remaining amount.

[Claim 3]

An image compression apparatus comprising:

an image compression means for compressing and encoding an image by using wavelet transform for frequency transform;

a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery; and

a first setting means for setting a number of taps of a wavelet filter used for the wavelet transform in accordance with the detected battery remaining amount.

[Claim 4]

An image compression apparatus comprising:

an image compression means for compressing and encoding an image by using wavelet transform for frequency transform;

a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery; and

a first setting means for setting a hierarchical level of the wavelet transform in accordance with the detected battery remaining amount.

[Claim 5]

The image compression apparatus according to claim 1, wherein

the first setting means sets the mode to a Lagrangian rate control mode when the battery remaining amount is above a predetermined reference value, and sets the mode to a plain rate control mode when the battery remaining amount is below the reference value.

[Claim 6]

The image compression apparatus according to claim 2, wherein the first setting means sets the mode to an overlap mode when the battery remaining amount is above a predetermined reference value, and sets the mode to a non-overlap mode when the battery remaining amount is below the reference value.

[Claim 7]

The image compression apparatus according to claim 3, wherein the first setting means sets the number of taps to 9*7 when the battery remaining amount is above a predetermined reference value, and sets the number of taps to 5*3 when the battery remaining amount is below the reference value.

[Claim 8]

The image compression apparatus according to claim 4, wherein the first setting means sets the hierarchical level to a 5-level when the battery remaining amount is above a predetermined reference value, and sets the hierarchical level to a 3-level when the battery remaining amount is below the reference value.

[Claim 9]

The image compression apparatus according to any one of claims 1 through 8 comprising a second setting means for setting the rate control mode or tiling mode, and number of taps or hierarchical level, regardless of the setting set by the first setting means.

[Claim 10]

The image compression apparatus according to any one of claims 1 through 9 comprising:

a variable voltage source for supplying voltage to the apparatus; and

a voltage control means for changing a voltage level in accordance

with a setting change carried out by the first, or second setting means.

[Claim 11]

The image compression apparatus according to any one of claims 1 through 9 comprising:

a clock generation means for generating a clock signal to be supplied to the apparatus; and

a frequency control means for changing the frequency of the clock signal in accordance with the setting change carried out by the first, or second setting means.

[Name of Document] Specification

[Title of the Invention] Image Compression Apparatus

[0001]

[Technical Field]

The present invention relates to an image compression apparatus for compressing and encoding image data.

[0002]

[Background Art]

A technique for suppressing power consumption in performing image compression processing by changing resolution or a frame rate of image data in accordance with a battery remaining amount, and changing a clock and power source voltage of a processing circuit based on the changed values is disclosed (refer to Japanese Patent document 1).

[0003]

In addition, JPEG 2000 is standardized as a new image compression technique.

[0004]

[Patent document 1] Japanese Patent Application Laid-Open No.2001-238189

[0005]

[Disclosure of the Invention]

[Problems to be Solved]

To reduce power consumption in performing processing to compress image data, particularly by using algorithms of JPEG 2000, not only changes in resolution and frame rate of the image data, but also changes in rate control (compression rate control of an image), tiling mode, and a number of taps of a wavelet filter and a hierarchical level used for wavelet transform, are effective. The technique disclosed in Japanese patent document 1 does not disclose control of the above elements to suppress power consumption, and reduction in power consumption is not enough.

[0006]

An object of the present invention is to sufficiently reduce power consumption in performing processing to compress and encode the image data.

[0007]

[Means for Solving the Problems]

The invention of claim 1 refers to an image compression apparatus including an image compression means for compressing and encoding an image, a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery, and a first setting means for setting a compression/encoding rate control mode in accordance with the detected battery remaining amount.

[0008]

Accordingly, electric power may be saved by rate control when the battery remaining amount becomes low.

[0009]

The invention of claim 2 refers to an image compression apparatus including an image compression means for dividing an image into a plurality of tiles and compressing and encoding an image in a hierarchical manner for each of the tiles, a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery, and a first setting means for setting a tiling mode in accordance with the detected battery remaining amount.

[0010]

Accordingly, electric power may be saved by tiling when the battery remaining amount becomes low.

[0011]

The invention of claim 3 refers to an image compression apparatus including an image compression means for compressing and encoding an image by using wavelet transform for frequency transform, a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery, and a first setting means for setting a number of taps of a wavelet filter used for the wavelet transform in accordance with the detected battery remaining amount.

[0012]

Accordingly, electric power may be saved by the number of taps for the wavelet filter when the battery remaining amount becomes low.

[0013]

The invention of claim 4 refers to an image compression apparatus including an image compression means for compressing and encoding an image by using wavelet transform for frequency transform, a detection means for detecting a battery remaining amount when a power supply of the apparatus is a battery, and a first setting means for setting a hierarchical level of the wavelet transform in accordance with the detected battery remaining amount.

[0014]

Accordingly, electric power may be saved by the hierarchical level of the wavelet transform when the battery remaining amount becomes low.

[0015]

The invention of claim 5 refers to the image compression apparatus according to claim 1, wherein the first setting means sets the mode to a Lagrangian rate control mode when the battery remaining amount is above a predetermined reference value, and sets the mode to a

plain rate control mode when the battery remaining amount is below the reference value.

[0016]

Accordingly, electric power may be saved by setting the plain rate control mode when the battery remaining amount becomes low.

[0017]

The invention of claim 6 refers to the image compression apparatus according to claim 2, wherein the first setting means sets the mode to an overlap mode when the battery remaining amount is above a predetermined reference value, and sets the mode to a non-overlap mode when the battery remaining amount is below the reference value.

[0018]

Accordingly, electric power may be saved by setting the non-overlap mode when the battery remaining amount becomes low.

[0019]

The invention of claim 7 refers to the image compression apparatus according to claim 3, wherein the first setting means sets the number of taps to 9*7 when the battery remaining amount is above a predetermined reference value, and sets the number of taps to 5*3 when the battery remaining amount is below the reference value.

[0020]

Accordingly, electric power may be saved by setting the number of taps of the wavelet filter to 5*3 when the battery remaining amount becomes low.

[0021]

The invention of claim 8 refers to the image compression apparatus according to claim 4, wherein the first setting means sets the hierarchical level to a 5-level when the battery remaining amount is above a predetermined reference value, and sets the hierarchical level to a 3-level when the battery remaining amount is below the reference value.

[0022]

Accordingly, electric power may be saved by setting the

hierarchical level of the wavelet transform to the 3-level when the battery remaining amount becomes low.

[0023]

The invention of claim 9 refers to the image compression apparatus according to any one of claims 1 through 8 including a second setting means for setting the rate control mode or tiling mode, and number of taps or hierarchical level, regardless of the setting set by the first setting means.

[0024]

Accordingly, electric power may be saved by the rate control, or the like when required, regardless of the battery remaining amount.

[0025]

The invention of claim 10 refers to the image compression apparatus according to any one of claims 1 through 9 including a variable voltage source for supplying voltage to the apparatus, and a voltage control means for changing a voltage level in accordance with the setting change carried out by the first, or second setting means.

[0026]

Accordingly, electric power may be saved by decreasing the voltage to be used.

[0027]

The invention of claim 11 refers to the image compression apparatus according to any one of claims 1 through 9 including a clock generation means for generating a clock signal to be supplied to the apparatus, and a frequency control means for changing the frequency of the clock signal in accordance with the setting change carried out by the first, or second setting means.

[0028]

Accordingly, electric power may be saved by reducing the frequency of the clock signal to be used.

[0029]

[Best Mode for Carrying out the Invention]

An embodiment of the present invention is described.

[0030]

Fig. 1 is a block diagram showing a schematic configuration of an image compression apparatus 1 according to an embodiment of the present invention. The image compression apparatus 1 compresses and encodes image data based on, for example, a JPEG 2000 algorithm. Therefore, compressed and encoded code streams are produced by dividing an image into a plurality of sub-regions called as tiles (tiling), and by compressing and encoding the image data in a hierarchical manner for each tile, using wavelet transform (DWT) for frequency transform.

[0031]

As shown in Fig. 1, an input part 2 accepts an image data input. The received image data is subjected to a tiling process and divided into a plurality of tiles at a predetermined tile size in a tiling processing part 3. A wavelet transform part 4 carries out the wavelet transform, using a 9*7 filter or a 5*3 filter. The wavelet transformed data is input to an entropy coder part 5 for per bit plane of each coefficient. The entropy coder part 5 performs entropy coding of the inputted wavelet coefficients. A rate control part 6 selectively discards codes produced through the entropy coding so that the codes become a predetermined code amount, and finally outputs code streams. The tiling processing part 3, wavelet transform part 4, entropy coder part 5, and rate control part 6 constitute an image compression means.

[0032]

A battery 7 is a power source for supplying electric power to the image compression apparatus 1. A variable voltage source 8 generates predetermined variable voltage from the battery 7, and supplies the variable voltage to the input part 2, tiling processing part 3, wavelet transform part 4, entropy coder part 5, and rate control part 6. The image compression apparatus 1 may be driven

by an AC power source, instead of the battery 7. A clock generation part 9 functions as a clock generation means, and supplies a clock signal to the tiling processing part 3, wavelet transform part 4, entropy coder part 5, and rate control part 6. A power source state detection part 10 functions as a detection means, and detects the remaining amount of the battery 7 using a known technique.

[0033]

An operation mode setting part 11 functions as a second setting means, and sets an operation mode (described later) of the image compression apparatus 1. A process mode setting part 12 functions as a first setting means, a voltage control means and a frequency control means, and sets process modes (described later) of each processing block for the tiling processing part 3, wavelet transform part 4, entropy coder part 5, and rate control part 6, respectively, based on the battery remaining amount detected by the power source state detection part 10 and/or the operation mode determined by the operation mode setting part 11. The process mode setting part 12 also sets a clock signal generated by the clock generation part 9, and a level of variable voltage output from the variable voltage source 8.

[0034]

Processing performed by the processing mode setting part 12 is described in detail. As shown in Fig. 2, the processing mode setting part 12 detects the battery remaining amount of the power source state detection part 10 (step S1), and compares the detection result with one or more predetermined threshold values (step S2). In the example, a threshold value is set to 1/2 of the full-charged state of the battery. If the detection result is greater than the threshold value, the processing mode setting part 12 determines that the battery remaining amount is "full". If the detection result is less than the threshold value, the processing mode setting part 12 determines that the battery remaining amount is "low". The processing mode setting part 12 further determines whether the

comparison result is changed, or not (the battery remaining amount greater than the threshold value becomes less than the threshold value, or the battery remaining amount less than the threshold value becomes greater than the threshold value) (step S3). If a change in the comparison result is determined, (step S3: Y), or if an operation mode different from the current operation mode is set by the operation mode setting part 11 (step S4: Y), appropriate table data is selected from a table 21 described later (step S5), processing modes of each processing block for the tiling processing part 3, wavelet transform part 4, entropy coder part 5 and rate control part 6 are newly set based on the table data, and a clock signal generated by the clock generation part 9 and a power source voltage level output from the variable voltage source 8 are newly set (step S6).

[0035]

Fig. 3 is an explanation diagram of the table 21. In the table 21, a process mode, a clock signal, and output voltage are registered in association with three power source states including a case that an AC power source is used in the image compression apparatus 1 ("AC"), a case that the battery 7 is used and the remaining amount of the battery is greater than the threshold value (1/2 of the full-charged state)("full"), a case that the battery 7 is used and the remaining amount of the battery is less than the threshold value ("low"). In addition, three operation modes including an "ordinary mode", "power-saving mode 1", and " power-saving mode 2" are registered. The "ordinary mode" corresponds to "AC", "power-saving mode 1" corresponds to "full", and "power-saving mode 2" corresponds to "low".

[0036]

In a case of the "AC" or the "ordinary mode", a processing mode for the tiling processing part 3, that is, tiling, is set to the overlap mode, a processing mode for the wavelet transform part 4, that is, a number of taps of the filter used for the wavelet transform,

is set to 9*7, and a processing mode for the rate control part 6, that is, rate control (compression rate control for an image), is set to the Lagrangian rate control. In addition, a clock signal at the clock generation part 9 is set to a predetermined reference frequency (1/1 clock), and an output voltage of the variable voltage source 8 is set to 3.3V.

[0037]

In a case of the "full" or the " power-saving mode 1", in order to reduced power consumption, the rate control is set to the Lagrangian rate control for the case of "AC" or the "ordinary mode".

[0038]

In a case of the "low" or the "power-saving mode 2", in order to further reduce power consumption, tiling is set to the non-overlap mode, a number of taps of the wavelet transform filter is set to 5*3, and rate control is set to the plain rate control for the "full" or the "power-saving mode 1". Since the power consumption processing amount is reduced, the clock signal is set to 3/4 clock (3/4 of the predetermined reference frequency) and the power source voltage is decreased to 3.1V to reduced power consumption.

[0039]

A tiling operation performed by the tiling processing part 3 is described referring to Fig. 4. As shown in Fig. 4, the tiling processing part 3 divides an image into tiles 31 of a predetermined size. When the overlap mode is selected, in addition to the designated size, a portion that overlaps with peripheral tiles 31 for a predetermined pixel region is treated as a set of tile data (reference numeral 32 shows a data area in such a case). Accordingly, the data amount of per tile is increased, and the processing amount of data transfer or wavelet transfer is increased when compared to a case of divided tiles 31 without overlapping. As a result, the power consumption for processing is increased. However, if the overlapped tile region is not provided, dummy data needs to be

substituted for the pixel data located near the boundary of the tile 31 and required for wavelet transform. In such a case, when quantization is carried out, an error may occur in the pixel data near the tile boundary. Accordingly, the tile boundary becomes conspicuous. However, such a problem may be solved by performing filtering processing.

[0040]

The wavelet filters used in the wavelet transform part 4 is described. Fig. 5(a), and (b) show a filter of a tap number 9*7. For a high frequency component, the target pixel 41 and successive three pixels 42 through 44 and 46 through 48 on both sides of the target pixel 41 are processed, and data a-3 through a+3 of the pixels are subjected to multiplication and summation, using coefficients A1 through A7. For a low frequency component, the target pixel 41 and successive four pixels 42 through 45 and 46 through 49 on both sides of the target pixel 41 are processed, and data a-4 through a+4 of the pixels are subjected to multiplication and summation, using coefficients B1 through B9.

[0041]

Fig. 5(c), and (d) show a filter of a tap number 5*3. For a high frequency component, the target pixel 41 and the adjacent pixels 42 and 46 are processed, and data a-1 through a+1 of the pixels are subjected to multiplication and summation, using coefficients D1 through D3. For ae low frequency component, the target pixel 41 and successive two pixels 42 through 43 and 46 through 47 are processed, and data a-2 through a+2 of the pixels are subjected to multiplication and summation, using coefficients E1 through B5.

[0042]

In the 9*7 filter, totally sixteen times of multiplication and summation of the multiplication results are carried out. For the 5*3 filter, totally eight times of multiplication and summation of the multiplication results are carried out. Thus, an amount of arithmetic operation of the 9*7 filter is almost twice an amount

of the 5*3 filter.

[0043]

By reducing a number of hierarchical levels, he amount of arithmetic operation may be reduced. That is, as may be seen from wavelet coefficients shown in Fig. 6, in a case of 5-level (Fig. 6(b)), coefficients of 4HL, 4LH, 4HH, 5HL, 5LH, 5HH, and 5LL need to be calculated, and the amount of arithmetic operation become greater when compared to 3-level (Fig. 6(a)).

[0044]

Consequently, arithmetic processing amount of the 5*3 filter (3-level) is less than the 9*7 filter (5-level). Therefore, electric power used for the former processing may be greatly reduced.

[0045]

The plain rate control is described. Fig. 7 is a functional block diagram of a rate control part 6 when the plain rate control is carried out. As shown in Fig. 7, a code discard means 51 discards codes in a predetermined order so that the input code streams become a target code amount. A discard portion determination means 53 determines a portion of the code to be discarded by the code discard means 51 based on the data amount of the respective code portions, the table data of a discard order table 52 arranged in a preliminary determined order from the least visually significant data, and the target code amount. The code discard means 51 outputs remaining code streams in which codes are discarded. The Lagrangian rate control is well known (refer to Japanese Patent publication No. 3281423, if necessary), and therefore, detail descriptions are omitted.

[0046]

According to the image compression apparatus 1, when the battery remaining amount becomes low, the plain rate control and the non-overlap modes are set, a number of taps of the wavelet filter is set to 5*3, and a hierarchical level of the wavelet transform is set to 3-level. The voltage and frequency of the clock signal

used for such a case are also decreased. As a result, power consumption of the image compression apparatus 1 may be reduced.

[0047]

In addition, power consumption may be reduced regardless of the battery remaining amount by adjusting the rate control, etc. (step S4: Y, S5, and S6) when required, using the operation mode setting part 11.

[0048]

[Effects of the Invention]

The invention of claim 1, wherein power consumption may be reduced by rate control, when the battery remaining amount becomes low.

[0049]

The invention of claim 2, wherein the power consumption may be reduced by tiling, when the battery remaining amount becomes low.

[0050]

The invention of claim 3, wherein the power consumption may be reduced by a number of taps of a wavelet filter, when the battery remaining amount becomes low.

[0051]

The invention of claim 4, wherein the power consumption may be reduced by a hierarchical level of wavelet transform, when the battery remaining amount becomes low.

[0052]

The invention of claim 5 according to the invention described in claim 1, wherein the power consumption may be reduced by setting a plain rate control mode, when the battery remaining amount becomes low.

[0053]

The invention of claim 6 according to the invention described in claim 2, wherein the power consumption may be reduced by setting a non-overlap mode, when the battery remaining amount becomes low.

[0054]

The invention of claim 7 according to the invention described

in claim 3, wherein the power consumption may be reduced by setting a number of taps of the wavelet filter to 5*3, when the battery remaining amount becomes low.

[0055]

The invention of claim 8 according to the invention described in claim 4, wherein the power consumption may be reduced by setting a hierarchical level of the wavelet transform to 3-level, when the battery remaining amount becomes low.

[0056]

The invention of claim 9 according invention described in any one of claims 1 through 8, wherein the power consumption may be reduced by rate control when necessary regardless of a battery remaining amount.

[0057]

The invention of claim 10 according to invention described in any one of claims 1 through 9, wherein the power consumption may be reduced by decreasing voltage to be used.

[0058]

The invention of claim 11 according to invention described in any on of claims 1 through 9, wherein the power consumption may be reduced by reducing frequency of the clock signal to be used.

[Brief Description of the Drawings]

[Fig. 1]

Fig.1 is a block diagram showing a schematic configuration of an image compression apparatus according to an embodiment of the present invention.

[Fig. 2]

Fig. 2 is a flowchart of processing performed by the image compression apparatus.

[Fig. 3]

Fig. 3 is a conceptual diagram of a table used by the image compression apparatus.

[Fig. 4]

Fig. 4 is an explanatory diagram showing a tiling operation performed by a tiling processing part.

[Fig. 5]

Fig. 5 is an explanatory diagram showing a 9*7 tap filter, and a 5*3 tap filter.

[Fig. 6]

Fig. 6 is an explanatory diagram showing wavelet coefficients of a 3-level, and a 5-level.

[Fig. 7]

Fig. 7 is a functional block diagram of a rate control part when plain rate control is performed.

[Reference Numerals]

1	Image compression apparatus
3~6	Image compression means
7	Battery
8	Variable voltage source
9	Clock generation means
10	Detection means
11	Second setting means
12	First setting means

[Name of Document] Abstract of the Disclosure

[Abstract]

[Objectives of the Invention]

To sufficiently reduce power consumption in performing compression and encoding of image data.

[Means for Achieving the Objectives]

A processing mode setting part 12 detects a battery remaining amount of a power source state detection part 10 (step S1), and compares the battery remaining amount with a threshold value. When the comparison result with the threshold value is changed, the processing mode setting part 12 selects appropriate table data, sets a processing mode of each processing block for a tiling processing part 3 through a rate control part 6 based on the table

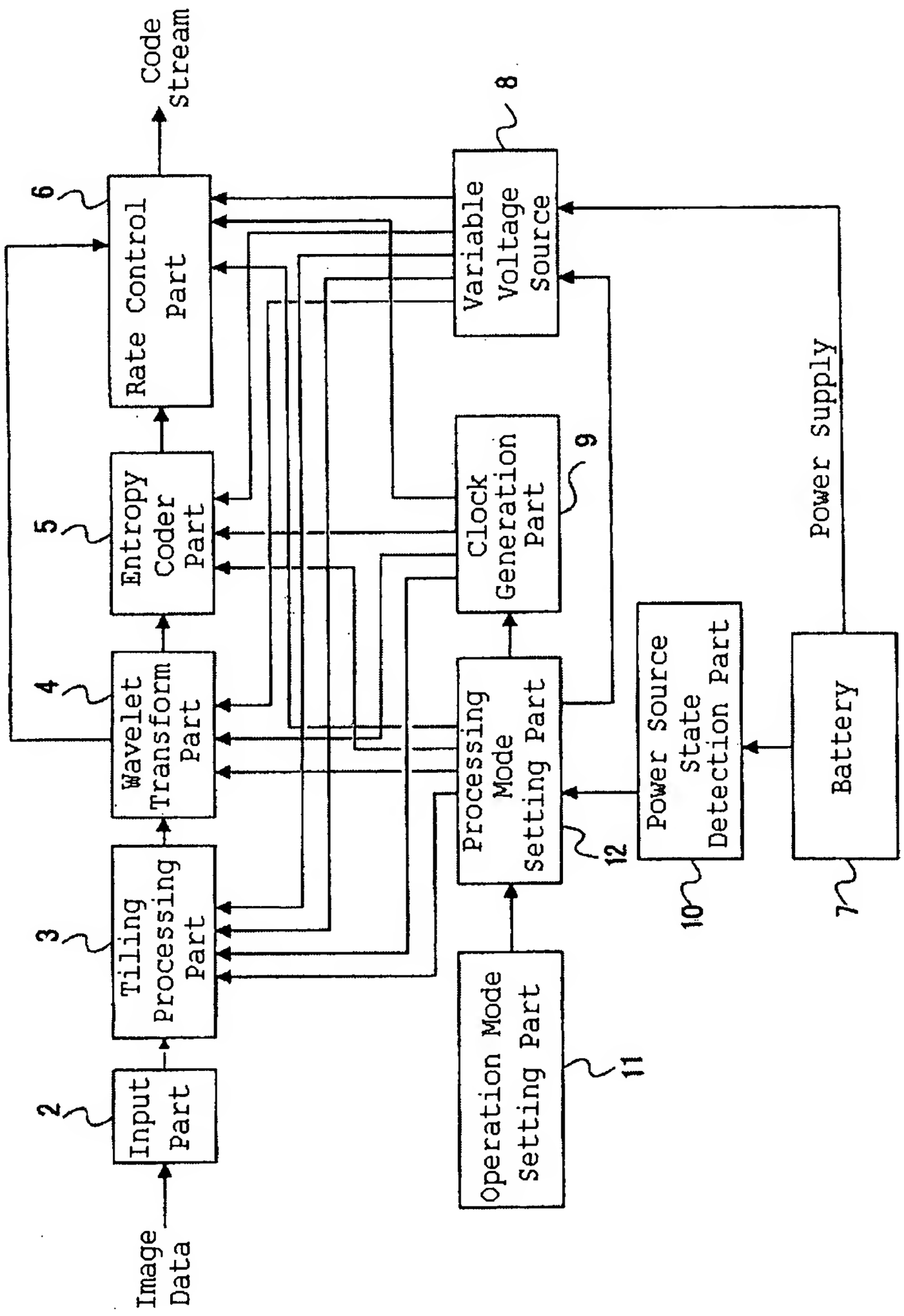
data, and newly sets a clock signal generated by a clock generation part 9 and a power source voltage level output from a variable voltage source 8.

[Selected Drawing]

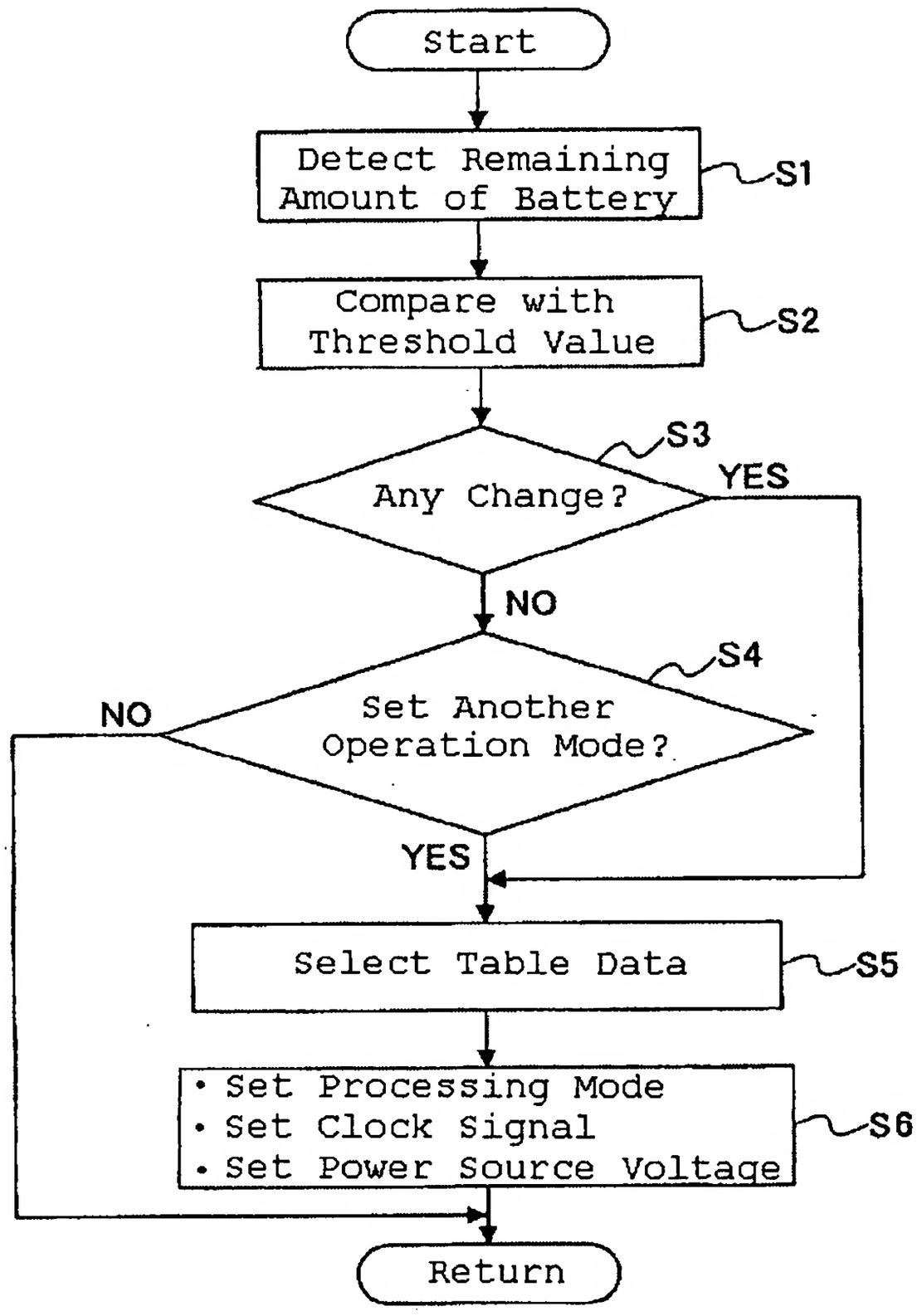
Fig. 1

[Name of Document]

[Fig. 1]



[Fig. 2]



[Fig. 3]

Power Source State (Operation Mode)	Processing Mode	Clock	Power Source Voltage
AC (Ordinary Mode)	Overlap 9*7 (5-Level) Lagrangian Rate Control	1/1 Clock	3.3V
Battery Full (Power-saving Mode 1)	Overlap 9*7 (5-Level) Plain Rate Control	1/1 Clock	3.3V No Power Supply For Lagrangian Rate Control
Battery Low (Power-saving Mode 2)	Non-overlap 5*3 (3-Level) Plain Rate Control	3/4 Clock	3.1V

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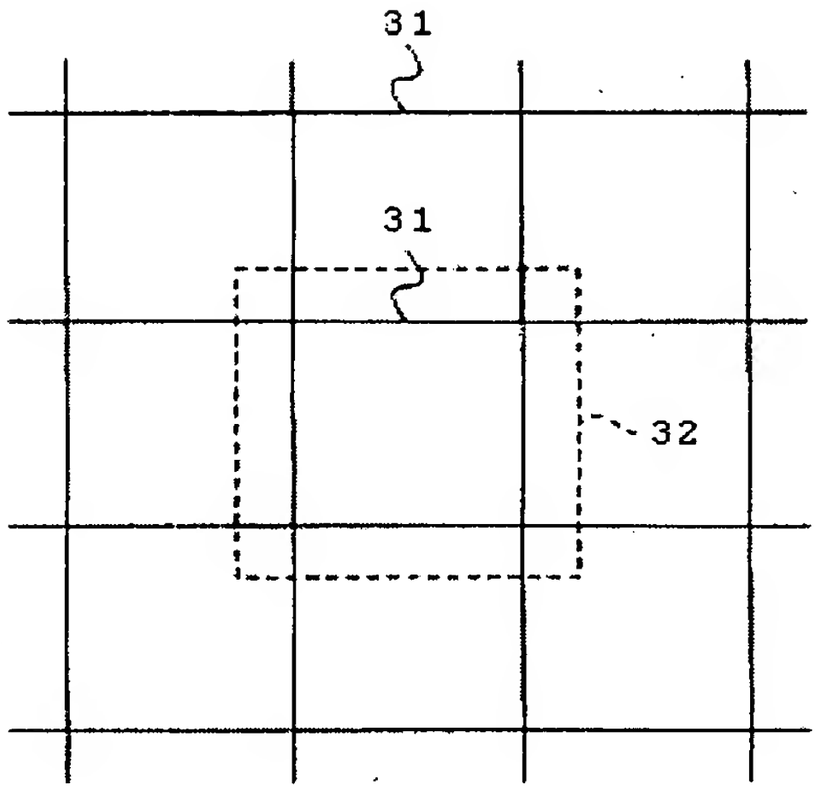
[Fig. 4]

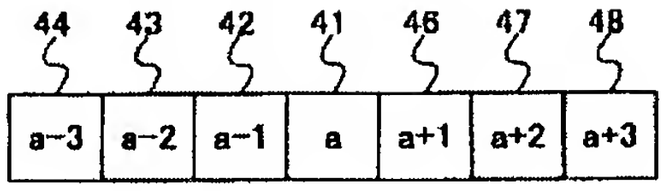


[Fig. 5]

(a)

9*7 Filter:

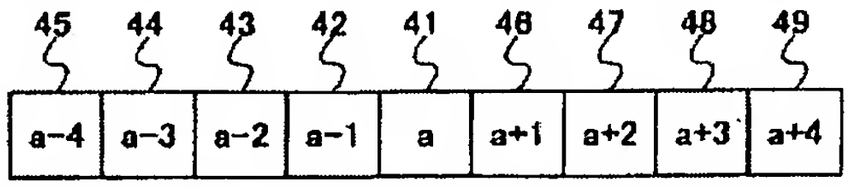
High Frequency Component



Coefficient = A1*a-3+A2*a-2+A3*a-1+A4*a+A5*a+1+A6*a+2+A7*a+3

(b)

Low Frequency Component

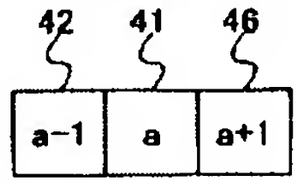


Coefficient = B1*a-4+B2*a-3+B3*a-2+B4*a-1+B5*a+B6*a+1+B7*a+2+B8*a+3+B9*a+4

(c)

5*3 Filter:

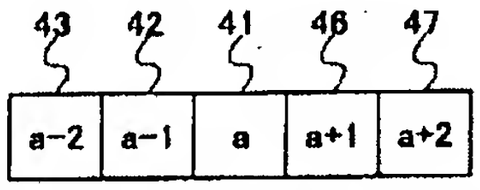
High Frequency Component



Coefficient = D1*a-1+D2*a+D3*a+1

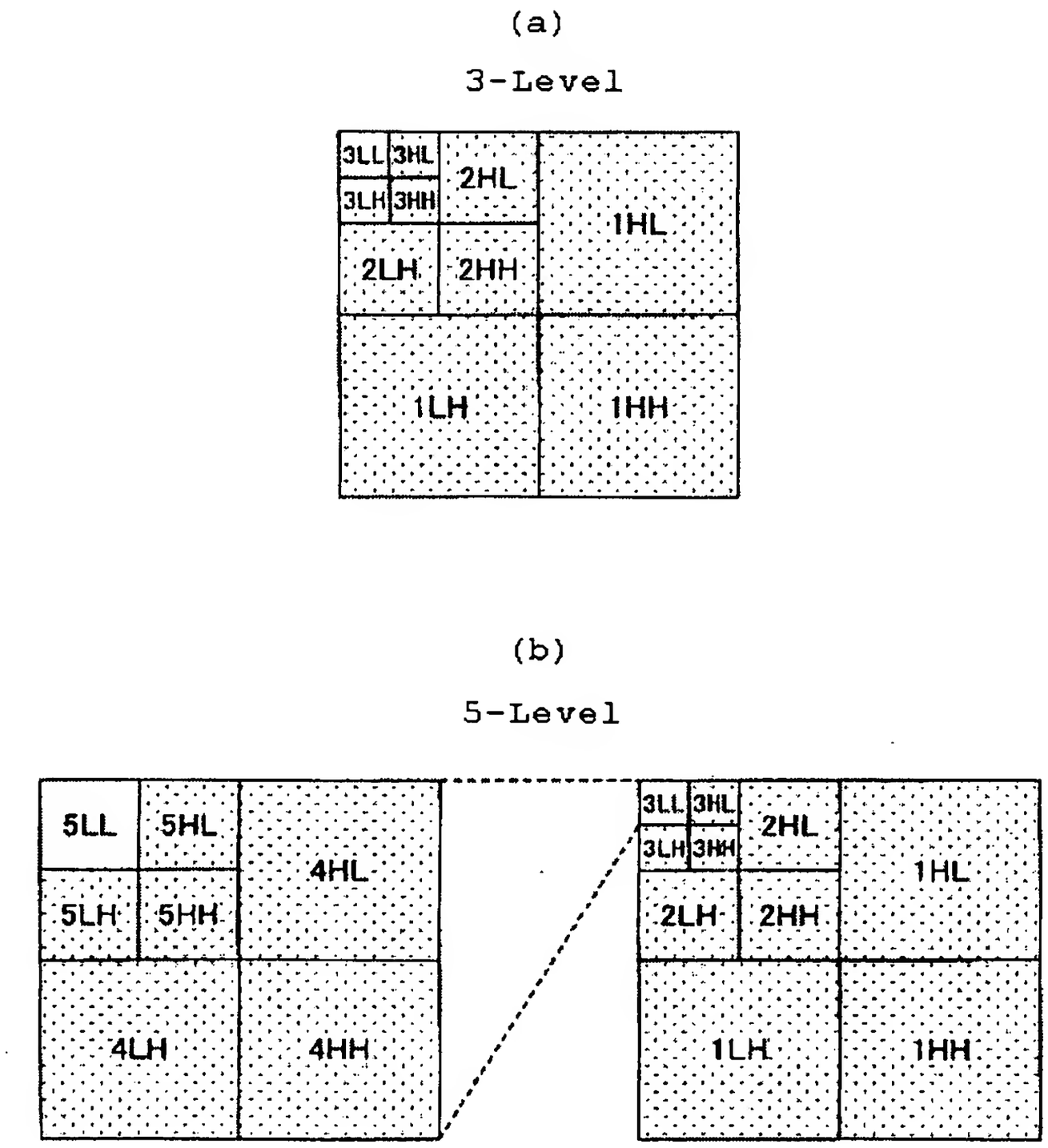
(d)

Low Frequency Component

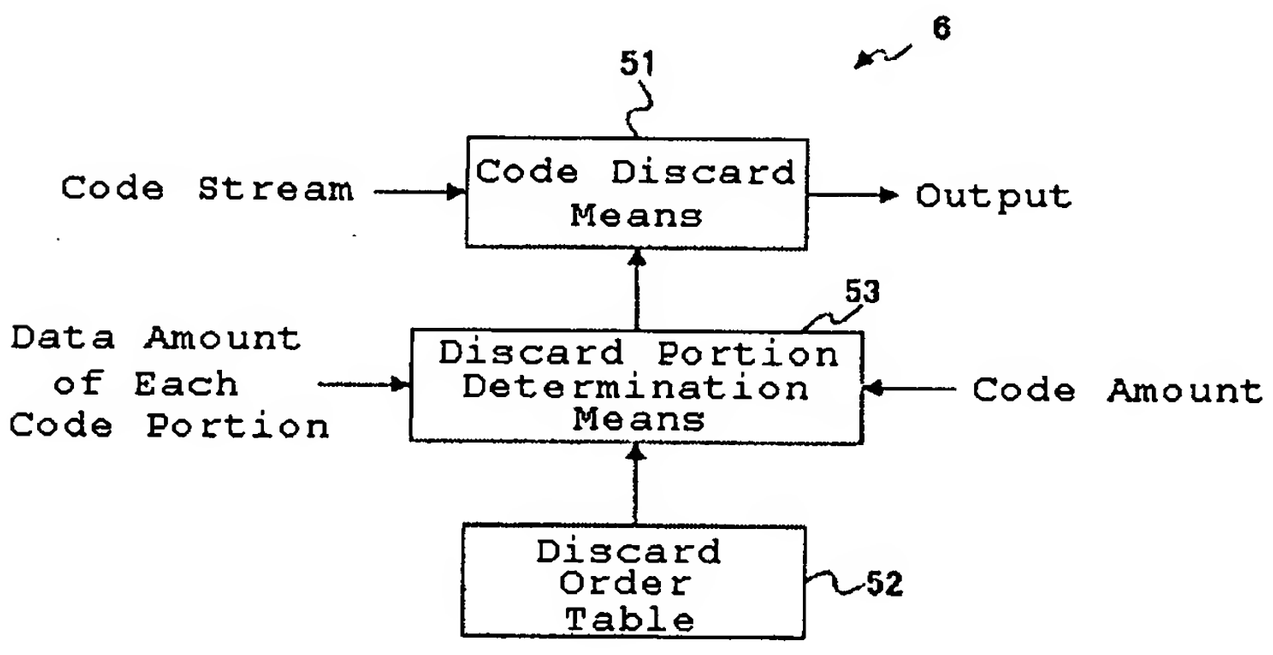


Coefficient = E1*a-2+E2*a-1+E3*a+E4*a+1+E5*a+2

[Fig. 6]


(a)
3-Level
3LL
3HL
3LH
3HH
2HL
2LH
2HH
1HL
1LH
1HH
(b)
5-Level
5LL
5HL
5LH
5HH
4HL
4LH
4HH
3LL
3HL
3LH
3HH
2HL
2LH
2HH
1HL
1LH
1HH

[Fig. 7]


6
51
Code Stream
Code Discard Means
Output
53
Data Amount of Each Code Portion
Discard Portion Determination Means
Code Amount
Discard Order Table
52

5